IN THE CLAIMS:

We claim:

1. A memory array system comprising a plurality of memory cells arranged in a data array and wordline decoding circuitry for receiving a control signal for activating one of a single wordline and at least two wordlines of a plurality of wordlines traversing the plurality of memory cells during a data array accessing cycle.

2. The memory array system according to Claim 1, wherein said wordline decoding circuitry includes a pre-decoder circuit having a logic circuit for receiving the control signal and two logic inputs and outputting at least one wordline selection signal to wordline activating means.

3. The memory array system according to Claim 2, wherein said logic circuit includes two pairs of transmission gates and first and second NAND logic gates coupled to a respective pair of the two pairs of transmission gates, wherein each pair of transmission gates receives the control signal, one of the two logic inputs, and an inverse input of one of the two logic inputs.

4. The memory array system according to Claim 2, wherein said wordline activating means includes a first and a second line shifter and a wordline driver circuit having wordline drivers for activating a respective one of the plurality of wordlines.

5. The memory array system according to Claim 1, wherein said wordline decoding circuitry includes means for interchanging at least a group of the plurality of memory cells coupled to at least one activated wordline between single-cell and twin-cell array operation.

6. The memory array system according to Claim 5, wherein in said single-cell array operation data is stored in a single-cell array format and in said twin-cell array operation data is stored in a twin-cell array format.

7. The memory array system according to Claim 1, wherein said plurality of wordlines have an interleaved arrangement, wherein a group of wordlines of the plurality of wordlines are activated from a left side of the data array and a group of wordlines of the plurality of wordlines are activated from a right side of the data array.

8. The memory array system according to Claim 1, further comprising an address directory register for storing the address of each memory cell operating in a single-cell array operation and the address of each memory cell operating in a twin-cell array operation.

9. The memory array system according to Claim 1, wherein the memory cells are selected from the group consisting of DRAM and TRAM cells.

10. A memory array system comprising a plurality of memory cells arranged in an array, and a memory controller having means for accessing an address directory register storing an address and a status of each of the plurality of memory cells, said memory controller further having means for determining the address and status of at least one of the plurality of memory cells and means for activating one of a single wordline and at least two wordlines of a plurality of wordlines traversing the plurality of memory cells during a data array accessing cycle.

11. The memory array system according to Claim 10, wherein said memory controller further comprises means for updating the status of the at least one of the plurality of memory cells.

12. The memory array system according to Claim 10, further comprising means for interchanging at least one of the plurality of memory cells between single-cell and twin-cell array operation, wherein in said single-cell array operation data is stored in a single-cell array format and in said twin-cell array operation data is stored in a twin-cell array format.

13. The memory array system according to Claim 10, wherein the memory cells are selected from the group consisting of DRAM and TRAM cells.

14. Wordline decoding circuitry for controlling dual wordline activation for a memory array, said wordline decoding circuitry comprising:

circuitry for receiving at least one control signal; and

wordline activation circuitry for enabling or disabling dual wordline activation according to said received at least one control signal.

15. Wordline decoding circuitry according to Claim 14, wherein said wordline activation circuitry includes circuitry for interchanging at least one of a plurality of memory cells of the memory array between single-cell and twin-cell array operation, wherein in said single-cell array operation data is stored in a single-cell array format and in said twin-cell array operation data is stored in a twin-cell array format.

16. The memory array system according to Claim 15, wherein the memory cells are selected from the group consisting of DRAM and TRAM cells.

17. A method for processing data in a memory system comprising a plurality of memory cells arranged in an array, said method comprising the steps of:

storing data within the array in a single-cell array format during a first operating mode of said memory system;

storing data within the array in a twin-cell array format during a second operating

mode of said memory system; and

converting data from said single-cell array format to said twin-cell array format by a method comprising the steps of:

activating a first wordline traversing the array;

reading data stored within a first group of the plurality of memory cells of the array which are coupled to the first wordline to corresponding sense amplifiers; and

activating at least a second wordline traversing the array to write the data from the corresponding sense amplifiers to a second group of the plurality of memory cells of the array.

18. A method for processing data in a memory system comprising a plurality of memory cells arranged in an array, said method comprising the steps of:

storing data within the array in a single-cell array format during a first operating mode of said memory system;

storing data within the array in a twin-cell array format during a second operating mode of said memory system; and

converting data from said twin-cell array format to said single-cell array format by a method comprising the steps of:

activating at least a first wordline traversing the array;

reading data stored within a first group of the plurality of memory cells of the array which are coupled to the at least first wordline to corresponding sense amplifiers; and

activating a second wordline traversing the array to write data from the corresponding sense amplifiers to a second group of the plurality of memory cells of the array.

19. A method for converting data from a single-cell array format to a twin-cell array format, said method comprising the steps of:

activating a first wordline traversing a data array;

reading data stored within a first group of cells of the data array which are coupled to

the first wordline to corresponding sense amplifiers; and

activating at least a second wordline traversing the data array to write the data from the corresponding sense amplifiers to a second group of cells of the data array.

20. A method for converting data from a twin-cell array format to a single-cell array format, said method comprising the steps of:

activating at least a first wordline traversing a data array;

reading data stored within a first group of cells of the data array which are coupled to the at least first wordline to corresponding sense amplifiers; and

activating a second wordline traversing the data array to write data from the corresponding sense amplifiers to a second group of cells of the data array.